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LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035Date June 16, 2005Number of pages including cover sheet 2

To: US PTO

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TC 2825

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REMARKS:

☐ Urgent☐ For your review☒ Reply ASAP☐ Please comment

Application Number: 10/697,357
Filing date: October 29, 2003
First named inventor: Viswanathan Lakshmanan et al.
Attorney docket number: 03-1772 / 81610

Transmitted herewith for filing via facsimile:

- Status Request Letter

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**In re Application of :**

Viswanathan Lakshmanan et. al.

Serial No. :

10/697,357

Filed :

October 29, 2003

For :Method Of Partitioning An
Integrated Circuit Design For
Physical Design Verification**RECEIVED
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JUN 16 2005

Examiner :**Atty Docket :** 81610 / 03-1772**STATUS REQUEST**Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the
status notification to the address stated below.LSI Logic Corporation
1621 Barber Lane, MS D-106
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Respectfully submitted,



Timothy Croll, Ph: [+1] 408-433-7191

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